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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/682,827	10/23/2001	Ming-Dou Ker	NAUP0324USA	6934

27765 7590 04/06/2004

NAIPO (NORTH AMERICA INTERNATIONAL PATENT OFFICE)
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
KITOV, ZEEV	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 04/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/682,827	KER ET AL.	
	Examiner	Art Unit	
	Zeev Kitov	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 18, 34, 36 - 39, 44 - 55* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 18, 34, 36 - 39, 44 - 55* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Examiner acknowledges a submission of the amendment and arguments filed on February 2, 2004. Claims 19 – 33, 35 and 40 – 43 are deleted; Claims 6, 34 and 44 are substantially amended. Amended Abstract is approved. Applicant's arguments have been carefully considered but have been found unpersuasive. Following is the Claims rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1- 5, 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ker 1 et al. (US 5,576,557) in a view of Smith (US 6,049,119).

Ker 1 et al. disclose most of the Claim 1 elements including an ESD protection circuit having an I/O pad and an internal circuit (elements 2 and 3 in Fig. 1), a Vss and a Vdd power terminals, a first ESD-detection circuit connected between the I/O buffering pad and the Vss power terminal (element M2 in Fig. 1); a P-type silicon controlled rectifier (elements Q3 and Q4 in Fig. 1) including a first lateral silicon controlled rectifier (SCR) and a P-type trigger node (node 18 in Fig. 1), an anode and a cathode of the P-STSCR being electrically connected to the I/O buffering pad and the Vss power terminal

respectively; a second ESD-detection circuit electrically connected between the I/O buffering pad and the Vdd power terminal (element M1 in Fig. 1); and an N-type silicon controlled rectifier including a second lateral SCR (elements Q1 and Q2 in Fig. 1) and an N-type trigger node (node 13 in Fig. 1), a cathode and an anode of the N-STSCR being electrically connected to the I/O buffering pad and the Vdd power terminal respectively.

However, they do not disclose the P-type and N-type substrates. The P-type and N-type trigger nodes were identified according to a polarity of triggering voltage. As to P-type and N-type substrates, according to Ker 1 et al., (col. 4, lines 10 - 16, col. 10, lines 1 – 8), the ESD protection circuit is compatible with N-type well/P-type substrate and P-type well/N-type substrate, as well as twin well fabrication. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Ker 1 et al. solution by using P-type or N-type substrate according to Ker 1 et al., because a criticality of selection of particular type of the substrate was not disclosed, and additionally, the reference states (col. 4, lines 10 - 16, col. 10, lines 1 – 8), it is not critical, a selection of particular type of the substrate is a matter of designer convenience, rather than element of a novelty.

Additionally, they do not disclose substrate-triggered ESD protection elements. Smith discloses the substrate-triggered ESD protection elements (element 13 in Fig. 3, col. 5, line 50 – col. 6, line 53). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Ker 1 et al. solution by adding the substrate-triggering according to Smith, because as

Smith states (col. 2, lines 12 – 25), the substrate-triggering helps to lower the trigger voltage, which as well known in the art is essential for protection circuits designed for use with low supply voltage.

Regarding Claim 2, Ker 1 et al. disclose the P-STSCR in the ESD protection circuit including a p-type substrate with N-wells (see Fig. 2), a first N-well diffusion region and a first P^+ diffusion region in P-type substrate used as the cathode of the P-STCR; and a second N^+ diffusion region and a second P^+ diffusion region (elements 28 and 27 in Fig. 2) in the N-well (element 23 in Fig. 2) used as the anode of the P-STCR, the second P^+ diffusion region, the N-well, the P-substrate and the first N^+ diffusion region forming the first lateral SCR.

Regarding Claim 3, Ker 1 et al. disclose a circuit wherein in response to a positive voltage pulse at the I/O buffering pad, the first ESD detection circuit produces a first trigger current flowing into the P-type trigger node of the P-STSCR triggering the first lateral SCR in the P-STSCR to enter a latch state, the latch state turning on the P-STSCR so that a current incurred from the positive voltage pulse is discharged to the Vss power terminal (col. 4, line17 – col. 7, line 54).

Regarding Claim 4, Ker 1 et al. disclose the circuit wherein the N-STSCR in the ESD protection circuit including a P-type substrate with N-wells (see Fig. 2), a first N^+ diffusion region and a first P^+ diffusion region in P-type substrate uses as the cathode of the N-STSCR; and a second N^+ diffusion region and a second P^+ diffusion region (elements 26 an 25 in Fig. 2) in the N-well (element 21 in Fig. 2) for use as the anode of

the N-STSCR, the second P^+ diffusion region, the N-well, the P-type substrate and the first N^+ diffusion region forming the second lateral SCR.

Regarding Claim 5, Ker 1 et al. disclose the circuit wherein in response to a negative voltage pulse at the I/O buffering pad, the second ESD detection circuit produces a second trigger current flowing into the N-type trigger node of the N-STSCR triggering the second lateral SCR in the N-STSCR to enter a latch state turning on the N-STSCR so that current incurred from the negative voltage pulse is discharged to the Vdd power terminal (col. 4, line17 – col. 7, line 54).

Regarding Claim 7, Ker 1 et al. disclose the circuit wherein the NMOS (element (element M2 in Fig. 1) enhances the first trigger current so as to accelerate the triggering of the P-STSCR.

Regarding Claim 9, Ker 1 et al. disclose the circuit wherein the PMOS (element M1 in Fig. 1) enhances the second trigger current so as to accelerate the triggering of the N-STSCR.

Claims 6, 8 and 10 - 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ker 1 et al. in a view of Ker 2 et al. (US 5,959,820). As was stated above, Ker 1 et al. disclose all the elements of Claim 1. However, regarding Claims 6 and 8, they do not disclose the first and second ESD detection circuits having a resistor, a capacitor, a zener diode, a diode string or an NMOS. Ker 2 et al. disclose the ESD detection circuit having the resistor and capacitor (elements R and C in Fig. 15a and 15b), the zener diode (shown in Fig. 16e), a diode string (shown in Fig. 16b) and NMOS

(part of element 206 in Fig. 16a and 16b). All these elements are well known and widely used in the ESD protection circuits. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Ker 1 et al. circuit by adding the resistor and capacitor, the zener diode or the diode string according to Ker 2 et al., because as well known in the art, presence of the RC element in the ESD detection circuit makes the ESD protection element reacting to a front edge of the ESD event and therefore faster than otherwise, while the zener diode or string of the diodes set a threshold of the SCR firing.

Regarding Claims 10, Ker 2 et al. disclose the fist ESD detection circuit including a third resistor with a third capacitor (elements R and C in Fig. 15a) a first inverter (element 206 in Fig. 15a), an input node of the first inverter electrically connected to the Vdd power terminal and the Vss power terminal through the third resistor and the third capacitor respectively, an output node of the first inverter electrically connected to the P-type trigger node of the P-STSCR (elements PCLSCR in Fig. 15a).

As per Claim 12, Ker 2 et al. disclose the fist ESD detection circuit including a third resistor with a fourth capacitor (elements R and C in Fig. 13a) a second inverter (part of element 204a in Fig. 13a), an input node of the first inverter electrically connected to the Vdd power terminal and the Vss power terminal through the third resistor and the third capacitor respectively, an output node of the first inverter electrically connected to the P-type trigger node of the N-STSCR (elements NCLSCR in Fig. 13a).

Regarding Claim 11, in the ESD protection circuit of Ker 1 et al. modified according to Ker 2 et al., when a positive ESD voltage pulse is applied to the I/O buffering pad, the first inverter (element 206 in Fig. 15a) is charged by the positive ESD voltage pulse to generate a third trigger current at the output node of the first inverter, the third trigger current flowing into the P-type trigger node of the P-STSCR (elements PCLSCR in Fig. 15a) to trigger the fist lateral SCR, the first lateral SCR entering a latch state in response to the third trigger current and quickly turning on the P-STSCR so that current incurred from the positive voltage pulse is discharged to the Vss power terminal.

Regarding Claim 13, in the ESD protection circuit of Ker 1 et al. modified according to Ker 2 et al., when a negative ESD voltage pulse is applied to the I/O buffering pad, the first inverter (part of element 204 in Fig. 13a) is charged by the positive ESD voltage pulse to generate a third trigger current at the output node of the first inverter, the third trigger current flowing into the P-type trigger node of the P-STSCR (elements NCLSCR in Fig. 13a) to trigger the fist lateral SCR, the first lateral SCR entering a latch state in response to the third trigger current and quickly turning on the N-STSCR so that current incurred from the positive voltage pulse is discharged to the Vdd power terminal.

Regarding Claim 14, it differs from Claim 1, rejected accordingly by its requirement of plurality of stacked SCR's replacing single SCR's and functional limitations for values of holding voltage levels. Ker 2 et al. disclose the first stacked SCR (elements PCLSCR in Fig. 15a) and the second stacked SCR (elements NCLSCR in Fig. 13a) both including a plurality of the same type SCR's.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Ker 1 et al. solution by replacing the single PSCR and NSCR by their stacked counterparts according to Ker 2 et al., because as Ker 2 et al. state (col. 3, lines 50 - 55), such solution has a high bypassing ability without latchup risk. The stacked LVTSCR can provide the CMOS IC with effective ESD protection but without accidental triggering on by the overshooting or undershooting noise pulses in the system applications.

As to the holding voltage levels, as well known the art, the threshold levels for switching devices should be such that an information signal can come through, while the noise is rejected. The recited noise rejection capabilities of the first and second stack of SCR's are common noise rejection requirements for the switching circuit. The SCR's are to be switched by the ESD detection signals, but must be immune to the noise. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Ker 1 et al. system by adding the requirement of values for the holding voltage levels to satisfy conditions of firing SCR by the detected ESD event voltage and being immune to the noise, since it is routine requirement in switching system design taught in College Electronic Design courses.

Regarding Claims 16 and 18, Ker 2 et al. disclose the plurality of diodes series connected with each P-SCR (elements D1 - Dn in Fig. 21b) and the plurality of diodes series connected with each N-SCR (elements D1 – Dn in Fig. 21a). A motivation for such modification of the primary reference was given above.

Regarding Claim 15, Ker 1 et al. disclose the P-STSCR in the ESD protection circuit including a p-type substrate with N-wells (see Fig. 2), a first N-well diffusion region and a first P^+ diffusion region in P-type substrate used as the cathode of the P-STCR; and a second N^+ diffusion region and a second P^+ diffusion region (elements 28 and 27 in Fig. 2) in the N-well (element 23 in Fig. 2) used as the anode of the P-STCR, the second P^+ diffusion region, the N-well, the P-substrate and the first N^+ diffusion region forming the first lateral SCR.

Regarding Claim 17, Ker 1 et al. disclose the circuit wherein the N-STSCR in the ESD protection circuit including a P-type substrate with N-wells (see Fig. 2), a first N^+ diffusion region and a first P^+ diffusion region in P-type substrate uses as the cathode of the N-STSCR; and a second N^+ diffusion region and a second P^+ diffusion region (elements 26 an 25 in Fig. 2) in the N-well (element 21 in Fig. 2) for use as the anode of the N-STSCR, the second P^+ diffusion region, the N-well, the P-type substrate and the first N^+ diffusion region forming the second lateral SCR.

Claim 44 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ker 3 et al. (US 6,144,542). Regarding Claim 44, Ker 3 et al. disclose an ESD-connection circuit for use in separated power rails, the separated power rails including a first Vss and a first Vdd power terminals (Vdd1 and Vss1 in Fig. 3), a second Vss and a second Vdd power terminals (Vdd2 and Vss2 in Fig. 3), a first core circuit connected between the first Vdd power terminal and the first Vss power terminal (circuit 1 in Fig. 2), a second core circuit connected between the second Vdd power terminal and the second Vss

power terminal (circuit 2 in Fig. 3), the ESD-connection circuit including: at least one ESD-detection circuit (ESD Detection Circuit in Fig. 11); a first sub ESD-connection circuit, a second sub ESD-connection circuit, a third sub ESD-connection circuit, and a fourth sub ESD-connection circuit (all are shown as elements A in Fig. 3, col. 5, lines 35 – 42). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Ker 3 et al. circuit by introducing the ESD-detection circuit according to Ker 3 et al., because as well known in the art, it increases sensitivity and eventually a speed of reaction and reliability of the ESD protection devices.

As to their connection, Ker 3 et al. discloses connection of the ESD protection elements between two different Vdd power supply lines (between Vdd1 and Vdd2, Vss1 and Vss2 in Fig. 2). As to the ESD protection circuit placement between Vdd and Vss, Examiner takes an Official Notice that in design of the ESD protection circuits, the ESD protection devices are routinely placed between any two terminals susceptible to the ESD event; the only practical limitation is due to saving equipment and cost. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Ker 3 et al. Fig. 3 according to Ker 3 et al. Fig. 2 teaching and according to recited rule of design by placing the Ker 3 et al. A elements in recited positions, because as Ker 3 et al. states (col. 2, lines 39 – 44, 60 – 63), positioning the ESD protection circuits in recited locations are necessary to conduct current between separated power lines to avert the ESD damage.

Claims 34, 36, 37, 39, 45 – 47, and 49 - 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ker 3 et al. in a view of Smith. Ker 3 et al. disclose following elements of the claim including power-rail ESD clamp circuit for use with mixed voltages; the circuit has Vss, the first Vdd and the second Vdd power terminals (elements Vss1, Vss2, Vdd1 and Vdd2 in Fig. 3); it further includes the first, second and third sub power rail ESD clamp circuits (elements A in Fig. 3), which further disclosed as having an ESD detection circuit (two NMOS transistors in Fig. 6A) and SCR (two SCR's shown in Fig. 6A) having two trigger nodes. As to their connection, Ker 3 et al. discloses connection of the ESD protection elements between two different Vdd power supply lines (between Vdd1 and Vdd2, Vss1 and Vss2 in Fig. 2). As to the ESD protection circuit placement between Vdd and Vss, Examiner takes an Official Notice that in design of the ESD protection circuits, the ESD protection devices are routinely placed between any two terminals susceptible to the ESD event; the only practical limitation is due to saving equipment and cost. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Ker 3 et al. Fig. 3 according to Ker 3 et al. Fig. 2 teaching and according to recited rule of design by placing the Ker 3 et al. An elements in recited positions, because as Ker 3 et al. states (col. 2, lines 39 – 44, 60 – 63), positioning the ESD protection circuits in recited locations are necessary to conduct current between separated power lines to avert the ESD damage.

However, regarding Claims 34 and 45, Ker 3 et al. do not disclose a substrate-triggered silicon controlled rectifier (STSCR. Smith discloses the substrate-triggered

ESD protection elements (element 13 in Fig. 3, col. 5, line 50 – col. 6, line 53). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Ker 3 et al. solution by adding the substrate-triggering according to Smith, because as Smith states (col. 2, lines 12 – 25), the substrate-triggering helps to lower the trigger voltage, which as well known in the art is essential for protection circuits designed for use with low supply voltage.

Regarding Claims 36, 37,46 and 47, Ker 3 et al. disclose an SCR as a P-type silicon controlled rectifier (PCLSCR) and the trigger node is a P-type trigger node (shown in Fig. 9). They further disclose an N-type silicon controlled rectifier (NCLSCR) and the trigger node is an N-type trigger node (shown in Fig. 10). As to the substrate triggering, it was addressed above.

Regarding Claims 39 and 49, Ker 3 et al. disclose a plurality of diodes series connected with the SCR's (elements D1 – Dn in Fig. 10)..

As per Claims 50 - 53, they introduce requirement of SCR's interconnecting different power supply lines and being connected between first and second Vdd lines and the second and the first Vss lines. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have been modified the Ker 3 et al. Fig. 2 circuit by replacing the diode strings by SCR elements according to Fig. 8 of Ker 3 et al., because the sub ESD connection circuits are replacement for upper and bottom strings of diodes (elements 500 in Fig. 2), they are to be connected between different power supplies, i.e. the first and the second Vdd lines in the higher voltage supply line and between the second and the first.

Regarding Claims 54 and 55, Ker 3 et al. disclose the ESD detection circuit being connected between the first Vdd and Vss power terminals (Fig. 9).

Claims 38 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ker 3 et al. in a view of Smith and further in a view of Russ et al. Claims 38 and 48 require SCR being a double-triggered switch. Russ et al. disclose the SCR switch as a double-triggered silicon controlled rectifier (shown in Fig. 3) and the DT-SCR has a P-type trigger node and an N-type trigger node (points of connection of S1 and S2 switches to the SCR in Fig. 3). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Ker 3 et al. solution by adding the double triggering feature, because as Russ et al. state (col. 1, lines 7 – 10), the double-triggering mechanism helps to achieve faster turn-on.

Response to Arguments

Applicant's arguments have been carefully considered but have been found unpersuasive. Applicant has failed to specifically point out any claim limitation that was not met by the recited prior art.

Applicant's argument 1 states that Ker 1 et al. devices 100 and 200 are two low voltage controlled rectifiers (LTVSCRs), and cannot be arbitrarily separated. Examiner has not suggested that these devices are to be separated.

Applicant's argument that the structure of Ker 1 et al. circuit is totally different from the design of independent ESD-detection circuit of the invention is unsubstantiated and unsupported by the claim language.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

The new ground of rejection is the Examiner Official Notice used only for rejection of substantially amended Claims 34 and 44. The other claims are rejected with the same Prior Art as in the previous Office Action.

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose telephone number is (703) 305-0759. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (703) 308-3119. The fax phone number for organization where this application or proceedings is assigned is (703) 972-9306 for all communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Z.K.
03/30/2004

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